

Zener Voltage Regulation and Thermal Resistance

The effective PN junction operating temperature for very low zener power levels and pulse test methods will approximate ambient temperature conditions (TA) as described in MCC Note C003. In such examples, zener voltage (VZ) regulation versus temperature is only affected by the ambient TA. However, most zener JEDEC "1N" diode registration types identified in the industry are specified for VZ at dc thermal equilibrium conditions at a given test current (IZT) and power. Their effective zener dc power (Vz (IZT) and self heating effects will often generate sustained internal PN junction temperatures operating at 30 (C or more above their case or lead temperatures. Test conditions for zener voltage are typically at 25% of full rated power.

The notable increases in internal PN junction operating temperature are due to zener package thermal resistance (R(JL or R(JC) from junction to lead or case. In addition, the lead or case temperature can typically run higher in value than ambient since there will be a finite amount of thermal resistance (R(LA or R(CA) between lead or case to ambient surroundings with typical heatsinking mounting conditions. All of the thermal resistance values expressed are in (C/W. As an example, the junction temperature change ((TJ) above TA for a lead mounted device can be determined by a cumulative thermal resistance effect (R(JL + R(LA) with the following:

$$(TJ = (Vz (IZ) ((R(JL + R(LA)$$

The thermal soak time for typical axial leaded zeners to achieve thermal equilibrium after power (Vz(IZ) is applied, approximates 20 seconds or

more. The VZ is directly affected by TJ. To calculate the (Vz generated by cumulative effects of zener temperature coefficient and thermal resistance heating effects starting at the time power is applied, then the (TJ may be used above with the methods described in MCC Note C003. This would then provide:

$$(Vz ((Vz (IZ) ((R(JL + R(LA) (((VZ (Vz)/100$$

For an example with positive (VZ, zener voltage will increase with applied power until thermal equilibrium is achieved. Pulse testing voltage at a few milliseconds on JEDEC "1N" zener diode types with automatic test equipment (for quick screening or incoming sample inspections) will differ from specified thermal equilibrium conditions for Vz voltage at IZT. Such test method differences are predictable for zener package designs of known thermal resistance when case or lead temperatures (at 3/8 inch lead length) are referenced near 25 (C with minimal R(LA. When applicable, correlation factors can reconcile the two test methods when pulse testing zeners instead of waiting for thermal equilibrium. This is perhaps one of the most frequently misunderstood characteristics of zeners when quickly screened or sample tested by users.

If the absolute value of junction temperature (TJ) needs to be determined, then add TA to the change in junction temperature (TA+(TJ), or:

$$TJ = TA + Vz (IZ) ((R(JL + R(LA)$$

Since most zeners are specified at thermal equilibrium conditions at IZT and TA of 25(C, the (VZ values of interest are primarily those caused by changes ((IZ and (TA) from these specified conditions. This can be

initially expressed in terms of (TJ as:
(TJ ((TA ((Vz((IZ)((R(JL+R(LA) .

The (VZ deviation from standard rated test conditions can then be similarly determined as:

$$(Vz (((VZ (Vz) [(TA (Vz((IZ)((R(JL + R(LA)] /100$$

.This latter equation also uses earlier procedures described in MCC Note C003.

The R(LA or R(CA dictated by mounting is usually much smaller and independent from the zener diode itself. There can be exceptions for poorly mounted zeners, particularly with higher power rated zeners of 3 or more watts. As power ratings increase, lower thermal resistance (R(JL or R(JC) designs are used requiring lower R(LA or R(CA mounting practices with adequate heatsinking. This is an essential consideration in overall thermal management design for diode lead or case temperature control. Zener diode products are usually derated in power with reference to lead or case temperatures (TL or TC) to ensure that maximum conditions are not exceeded for best voltage regulation and reliability.

A typical printed circuit board (PCB) can often exhibit a mounting thermal resistance (R(LA) to an axial lead or surface mount diode of 30 to 50 (C/W, unless further provisions are made for better heatsinking. This can be provided with larger copper foot print areas or runners, lower thermal resistance board material, or moving air to help dissipate heat by radiation and convection. For example, PCB design is critical to minimize TL on 5 watt rated zener diodes typically exhibiting 25 (C/W (R(JL) at the typical 3/8 inch (10mm) lead length. Zeners are usually derated from full power starting at lead (or case) mounting temperatures of 50 to 75(C. This is required to maintain junction temperature at or below 175 to 200(C as displayed in Figure 1.

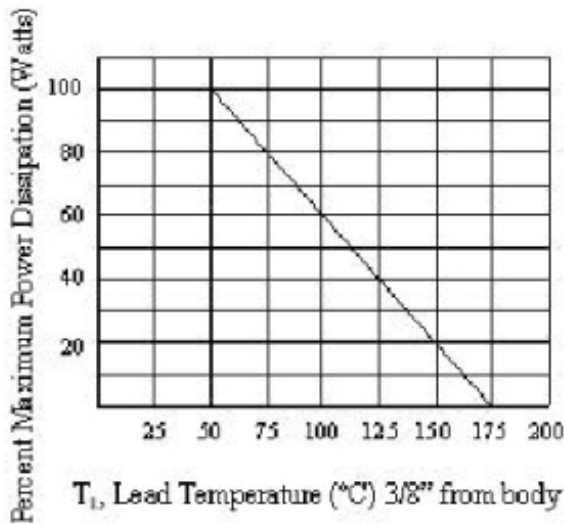


Figure 1. Zener Power Derating Curve

thermal management at higher power levels.

Understanding thermal resistance of zener diodes and their mounting requirements can be very important in a variety of applications for optimum voltage regulation and reliability with minimal operating temperatures. When very tight tolerance voltage regulation is required over a broad ambient operating temperature range, Zero-TC Reference Diodes may be needed. This subject will be described in subsequent issues of MCC Note.

INSERT FIGURE #1

Both the PC Board temperature (TB) and the TL of a zener dissipating power (Vz (Iz) is a similar calculation using the PCB footprint thermal resistance lead to ambient R(LA):

$$TB = TL = TA + Vz(Iz)(R(LA) .$$

The TB can also be directly measured at mounting locations with a small thermocouple after power and temperatures are stabilized. This may be the only means of determining local PCB footprint thermal resistance, or the cumulative temperature effects from other nearby components on a densely configured PC Board layout.

Since there are limitations to PCB mounting for minimal thermal resistance or optimum heat sinking, diodes rated well over 6 to 8 watts are generally found in other package configurations such as stud or flange mount designs in DO-4, DO-5, TO-3, TO-220, and other similar packages to achieve secure mounting to more substantial heat sinks. In such examples, there is significantly less mounting thermal resistance (often less than 1 (C/W) compared to PCBs. Despite the advantages of surface mount devices (SMDs) with less thermal resistance compared to conventional leaded packages, the PCB mounting itself ultimately becomes the limiting factor in