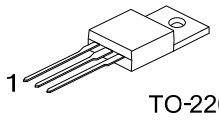
NJ5N80 POWER MOSFET

5.0A 800V N-CHANNEL POWER MOSFET

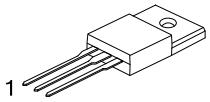
■ DESCRIPTION

The NJ5N80 is a N-channel enhancement mode power MOSFET. It use advanced technology to provide avalanche rugged technology and low gate charge.

It can be applied in high current, high speed switching, switch mode power supplies (SMPS), consumer and industrial lighting, DC-AC inverters for welding equipment and uninterruptible power supply(UPS).



TO-220

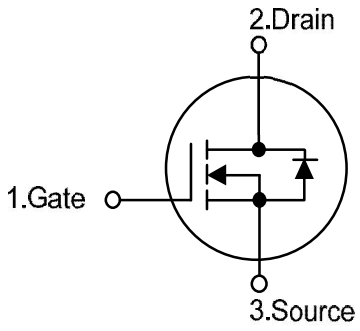


TO-220F

■ FEATURES

* V_{DS} = 800V
* I_D = 5.0A
* RDS(ON): 2.0 ohm(TYP.)
* Avalanche rugged technology
* Low input capacitance
* Low gate charge
* Application oriented characterization

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
NJ5N80-LI	TO-220	G	D	S	Tape Box
NJ5N80-BL	TO-220	G	D	S	Bulk
NJ5N80F-LI	TO-220F	G	D	S	Tube
NJ5N80A-LI	TO-251	G	D	S	Tube
NJ5N80D-TR	TO-252	G	D	S	Tape Ree
NJ5N80D-LI	TO-252	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

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■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{GS}=0		V_{DS}	800	V
Gate-Source Voltage			V_{GS}	±30	V
Drain-Gate Voltage	R_{GS}=20kΩ		V_{DGR}	800	V
Drain Current (Continuous)	Continuous		I_D	5.5	A
	Pulsed (Note 2)		I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)		E_{AS}	320	mJ
Power Dissipation		TO-220	P_D	125	W
		TO-220F		40	
Derating Factor		TO-220		1	W/°C
		TO-220F		0.32	
Junction Temperature			T_J	150	°C
Storage Temperature			T_{STG}	-55~150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by safe operating area.
3. Starting T_J=25°C, I_D=I_{AR}, V_{DD}=50V

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220	θ_{JC}	1	°C/W
	TO-220F		3.12	

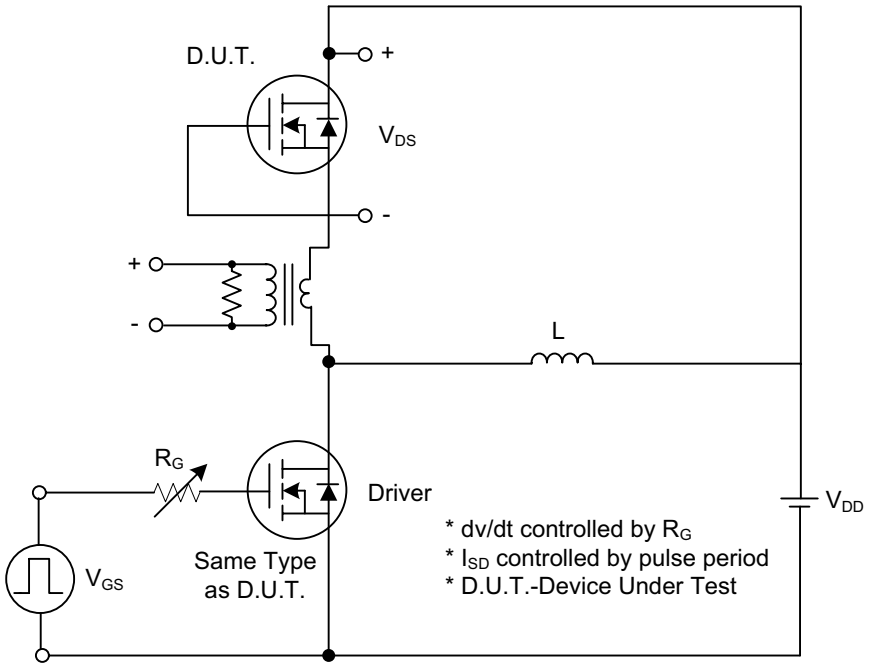
NJ5N80 POWER MOSFET

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

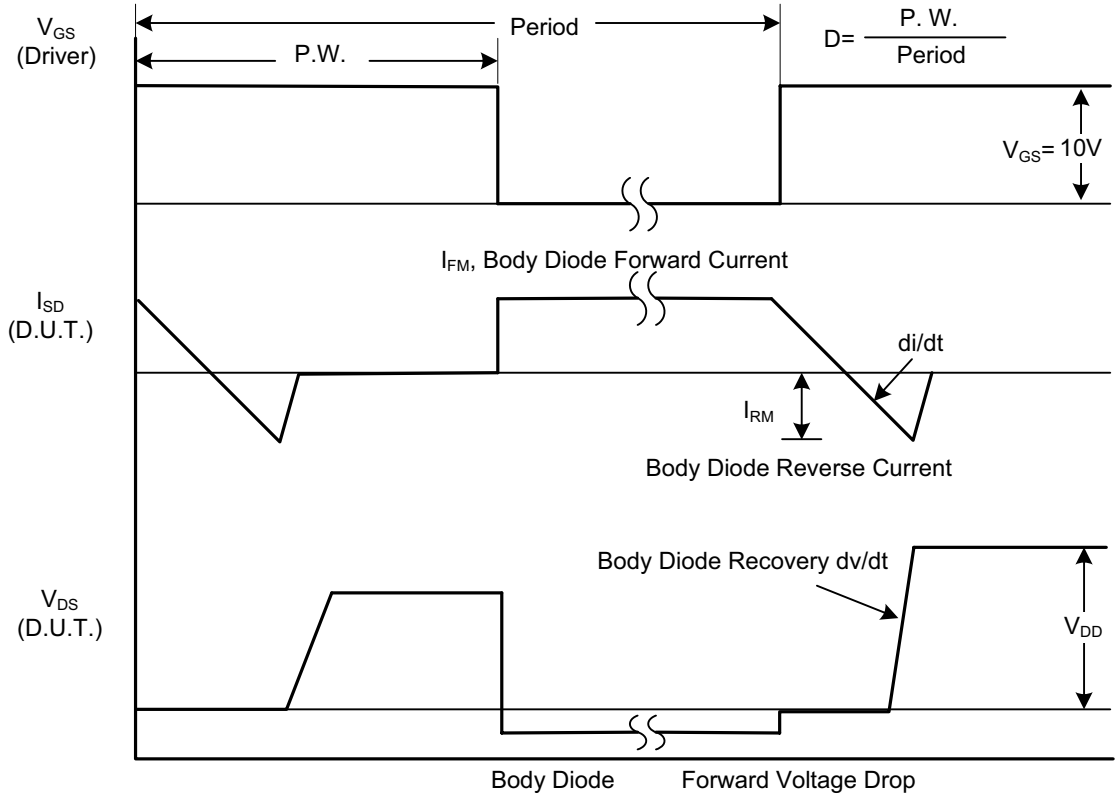
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	800			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=800V, V_{GS}=-0V			25	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V			+100	nA
	Reverse		V_{GS}=-30V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	3		5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=2.5A		2.0	2.5	Ω
			V_{GS}=10V, I_D=2.5A, T_C=100°C			4	
On State Drain Current		$I_{D(ON)}$	V_{DS}>$I_{D(ON)}$×$R_{DS(ON)}$max,V_{GS}=10V	5			A
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		1190	1450	pF
Output Capacitance		C_{OSS}			165	200	pF
Reverse Transfer Capacitance		C_{RSS}			70	85	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{GS}=10V, V_{DD}=500V, I_D=6A (Note 1, 2)		75	95	nC
Gate to Source Charge		Q_{GS}			9		nC
Gate to Drain Charge		Q_{GD}			33		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=400V, I_D=2.5A, R_G=50Ω		50	65	ns
Rise Time		t_R	V_{GS}=10V (Note 1, 2)		85	105	ns
Turn-OFF Delay Time		$t_{D(OFF)}$	V_{DD}=640V, I_D=5.5A, R_G=50Ω		120	150	ns
Fall-Time		t_F	V_{GS}=10V (Note 1, 2)		30	40	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	I_{SD}=5.5A, V_{GS}=0V			2	V
Reverse Recovery Time		t_{rr}	I_{SD}=5.5A,dI/dt=100A/μs, V_{DD}=80V,T_J=150°C (Note 1)		700		ns
Reverse Recovery Charge		Q_{RR}			7.7		nC
Reverse Recovery Current		I_{RRM}			22		A
Source-Drain Current		I_{SD}				5.5	A
Source-Drain Current (Pulsed) (Note 1)		I_{SDM}				20	A

Notes: 1. Pulsed: Pulse duration=300μs, duty cycle 1.5%.
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

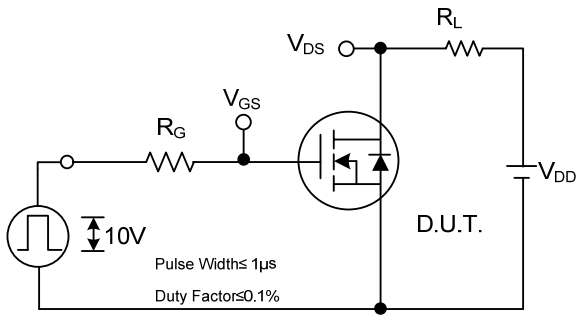


Peak Diode Recovery dv/dt Test Circuit

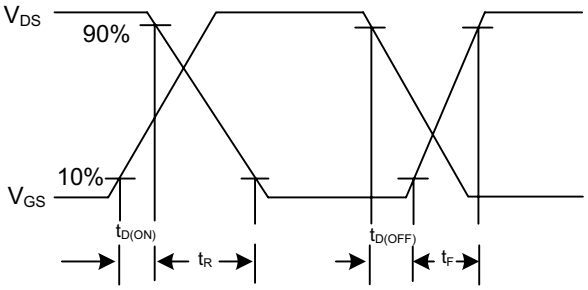


Peak Diode Recovery dv/dt Waveforms

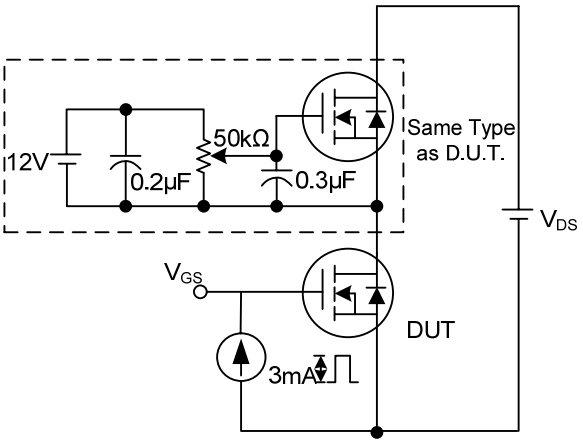
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



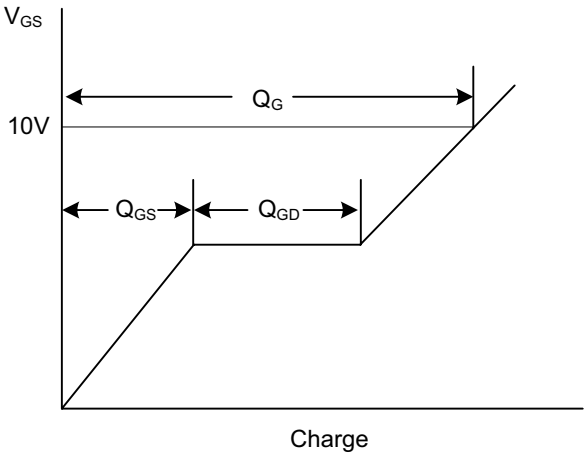
Switching Test Circuit



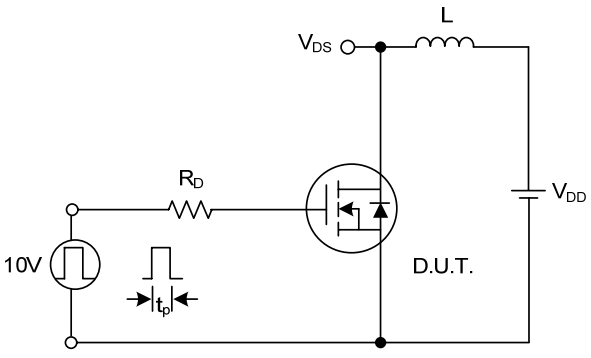
Switching Waveforms



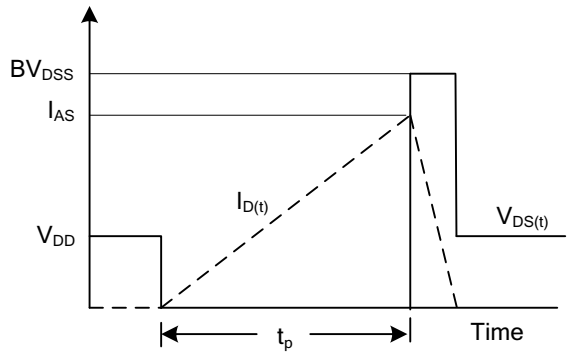
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms