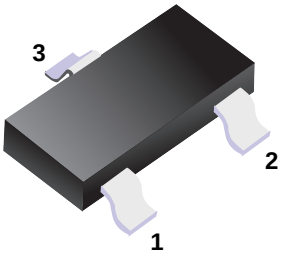
PCR404/406/408

Silicon Controlled Rectifiers

■ Features

- Sensitive gate silicon controlled rectifiers
- reverse blocking thyristors



1.Gate
2.Cathode
3.Anode

■ **Simplified outline(SOT-23)**

■ Absolute Maximum Ratings Ta = 25℃

Parameter		Symbols	Value	Units
Peak Repetitive Off-State Voltage Note4 (T_J = -40℃ to 110℃, Sine Wave, 50 to 60 Hz, Gate Open)	PCR404 PCR406 PCR408	V_{DRM}, V_{RRM}	200 400 600	V
On-State RMS Current (T_C= 80℃) 180℃ Conduction Angles		$I_{T(RMS)}$	0.5	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 25℃)		I_{TSM}	5	A
Circuit Fusing Considerations (t = 8.3ms)		I^2t	0.104	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1 μs)		P_{GM}	0.1	W
Forward Average Gate Power (t = 8.3ms)		$P_{G(AV)}$	0.1	W
Peak Gate Current – Forward (Pulse Width ≤ 1 μs)		I_{GM}	1	A
Peak Gate Voltage – Reverse (Pulse Width ≤ 1 μs)		V_{GRM}	5	V
Operating Junction Temperature Range		T_J	- 40 to + 110	℃
Storage Temperature Range		T_{STG}	- 40 to + 150	℃

■ Electrical Characteristics Ta = 25℃

Parameter		Symbols	Max	Units
Peak Forward or Reverse Blocking Current Note2 at V_D = Rated V_{DRM} and V_{RRM}, R_{GK} =1KΩ		I_{DRM}, I_{RRM}	10	μA
Peak Forward On-State Voltage Note1 at I_{TM} = 1 APeak		V_{TM}	1.7	V
Gate Trigger Current Note3 at V_{AK} = 7 V, R_L = 100 Ω		I_{GT}	200	μA
Holding Current Note2 at V_{AK} = 7 V, Initiating Current = 20 mA	T_C = 25 ŏ T_C=- 40 ŏ	I_H	5 10	mA
Latch Current at V_{AK} = 7 V, Ig = 200 μA	T_C= 25 ŏ T_C= - 40 ŏ	I_L	10 15	mA
Gate Trigger Voltage Note3 at V_{AK} = 7 V, R_L = 100 Ω	T_C= 25 ŏ T_C= - 40 ŏ	V_{GT}	0.8 1.2	V

Note:

1.Indicates pulse teat width ≤ 1 ms, duty cycle ≤1%

2.R_{GK} = 1 KΩ included in measurement

3.Does not include R_{GK} in measurement

4.V_{DRM} and V_{RRM} for all types can be applied on continous basis. Ratings apply for zero negative gate voltage; however,positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current sourse such that the voltage ratings of the devices are exceeded.

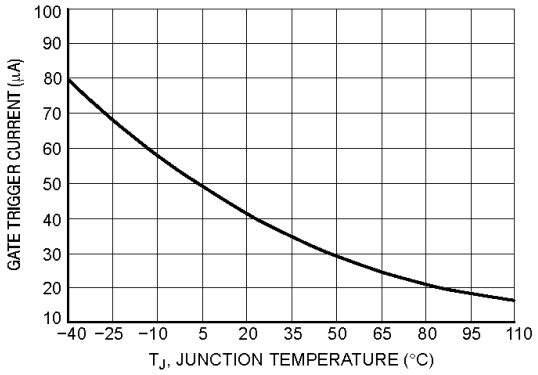


Figure 1. Typical Gate Trigger Current versus Junction Temperature

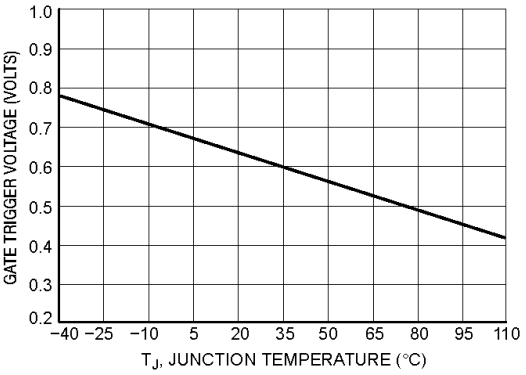


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

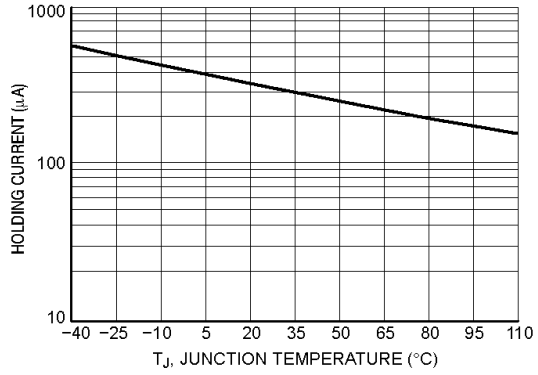


Figure 3. Typical Holding Current versus Junction Temperature

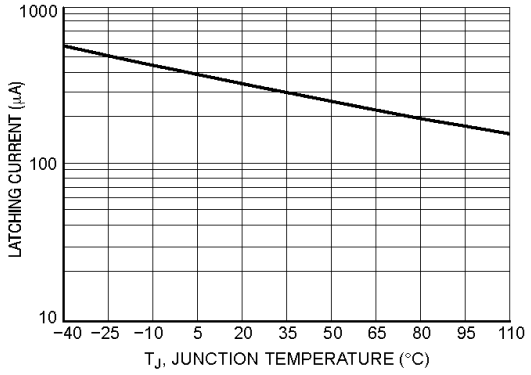


Figure 4. Typical Latching Current versus Junction Temperature